High-Performance 0.15-μm-Gate-Length pHEMTs Enhanced with a Low-Temperature-Grown GaAs Buffer

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Abstract - An improved GaAs power pHEMT is presented. The device utilizes a low-temperature-grown (LTG) GaAs buffer layer instead of the conventional-buffer layers commonly used by pHEMT manufacturers. When contrasted with identical devices using a conventional buffer, these LTG-buffered pHEMTs have shown a 45% increase in channel breakdown voltage, a 12% increase in power output, and a record 63% power-added efficiency at 20 GHz .

I. INTRODUCTION

GaAs submicrometer gate-length psuedomorphic-high-electron-mobility transistors (pHEMTs) are recognized for their ability to provide high output power and power-added efficiency at microwave and millimeter-wave frequencies. As applications continue to demand higher power output with high efficiency, more stringent requirements will be placed on higher power pHEMTs. While some of these requirements can be met by increasing the device gate-periphery to directly scale the power output, the gain degradation that occurs at high frequencies limits the applicability of this approach for high-efficiency applications. A better alternative that can provide improved power devices is to increase the useful device operating voltage by increasing the breakdown voltage without degrading the device power gain.

This paper describes a new approach to increasing the channel breakdown voltage of pHEMTs by introducing a low-temperature-grown (LTG) GaAs buffer layer in the device layer structure. The unique properties of this material make it superbly suited to enhance breakdown voltage, provide higher output power, and enhance the power-added efficiency of pHEMTs[1]. This work represents the first successful demonstration of LTG GaAs in a pHEMT structure. The LTG GaAs buffered pHEMTs reported in this paper have achieved a 45% increase in the channel breakdown voltage, a 12% increase in the power output, and an 8-percentage-point increase in the device power-added efficiency when contrasted with identical but conventional-buffered pHEMTs at 20 GHz. The dc characteristics and the RF performance of these enhanced power devices are described.

II. LTG GaAs Buffered pHEMTs

Submicrometer gate-length pHEMTs, like other GaAs-based metal-semiconductor field-effect transistor (MESFET) devices, exhibit a number of problems that are attributed to the semi-insulating GaAs substrate. In microwave power applications these include low drain-source breakdown voltage, low RF gain under high power operating conditions, and poor pinch off characteristics. Some of these problems occur because of currents which propagate from the drain to source within the semi-insulating region below the conducting layers. These effects are particularly important in devices with

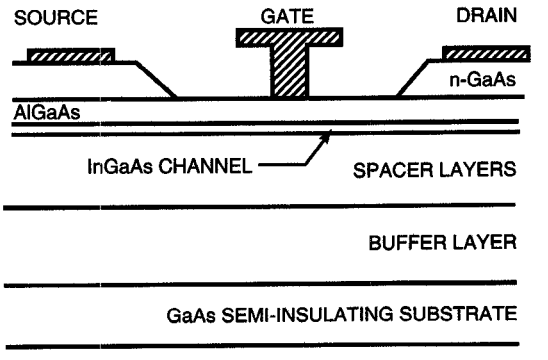

Fig. 1 Cross-sectional view of the basic LTG GaAs buffered pHEMT structure.

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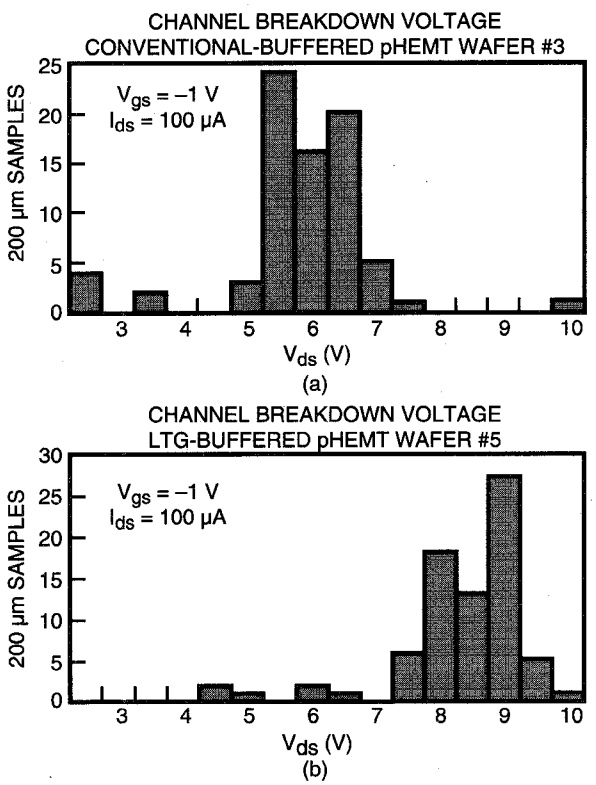

Fig. 2 A histogram of the channel breakdown voltage distribution for (a) a conventional-buffered and (b) LTG-buffered pHEMT wafer.

sub-micrometer gate-lengths and operating with large drain voltages. In order to alleviate these effects, a buffer layer is often inserted between the active layer (i.e. channel) and the substrate. A number of buffer layers, including undoped GaAs, AlGaAs, and superlatice (AlGaAs/GaAs) buffers are used by device manufacturers. However, these layers have provided limited success in mitigating the problems outlined above.

Low-temperature-grown GaAs is a material deposited by molecular beam epitaxy (MBE) at relatively lower substrate temperatures (~200 C) than those typically used for the growth of high-quality conducting GaAs (~ 600 C). The low temperature growth conditions result in a unique combination of large breakdown fields (~5 x 10 5 V/cm), high resistivity (~106 ohm-cm), high photoexcited-carrier mobility (200 cm2/V-s), and extremely short photoexcited-carrier lifetime (150 fs) that are particularly well-suited for buffer layers in power devices.[1-3] When used as a buffer layer in MESFET and MISFET devices, this material has demonstrated improved confinement of the drain-source current in the channel and dramatically reduced short-channel effects in submicrometer-gatelength MESFETs. In order to demonstrate the improvements that an LTG GaAs buffer might provide for high-performance submicrometer gate-length pHEMTs, a collaborative effort was undertaken with Martin Marietta under subcontract to Lincoln Laboratory to demonstrate LTG GaAs buffered pHEMT devices. A program was structured where pHEMT material layers containing an LTG GaAs buffer would be grown at the materials science laboratory of each facility using molecular-beam-epitaxy (MBE) on a 3-inch MOD GEN II MBE system. Two wafers from each facility were processed in Martin Marietta's pHEMT fabrication line; one control wafer, containing a conventional super-lattice buffer, and one wafer containing an LTG GaAs buffer layer. Fig. 1 illustrates the basic layer structure used for the LTG GaAs buffered pHEMTs. Devices consisting of gate-peripheries ranging from 200 μm to 4 mm with 0.15 μm gate lengths were contained on the mask set.

III. WAFER dc-CHARACTERISTICS

Four 3-inch pHEMT wafers were processed to completion for this demonstration. Using an Alessi 4500 semiautomatic wafer probe station, the dc-characteristics of 200 μm and 400 μm total gate-periphery devices from the LTG-buffered and the control wafers were measured. Measurements included dc-IV characteristics, dc-transconductance as a function of gate bias for varying drain voltage, I_{max}, I_{dss}, pinchoff voltage, gate-source breakdown voltage, gate-drain breakdown voltage, and channel breakdown voltage. In total approximately 3000 devices were sampled on each wafer.

One of the most important parameters for evaluating power output performance improvements of high-efficiency pHEMTs is the measurement of channel breakdown voltage. Since these devices are usually biased near pinch-off for highest power-added efficiency tuning, the drain-source breakdown at pinchoff becomes a useful measure of power performance improvement. To evaluate the improvement in channel breakdown, a sample of approximately 100 devices from an LTG-buffered wafer

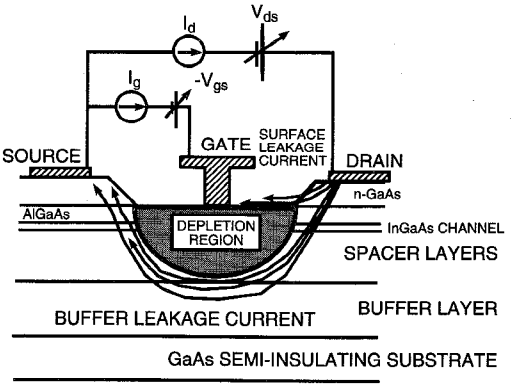

Fig. 3 Measurement of the buffer leakage current.

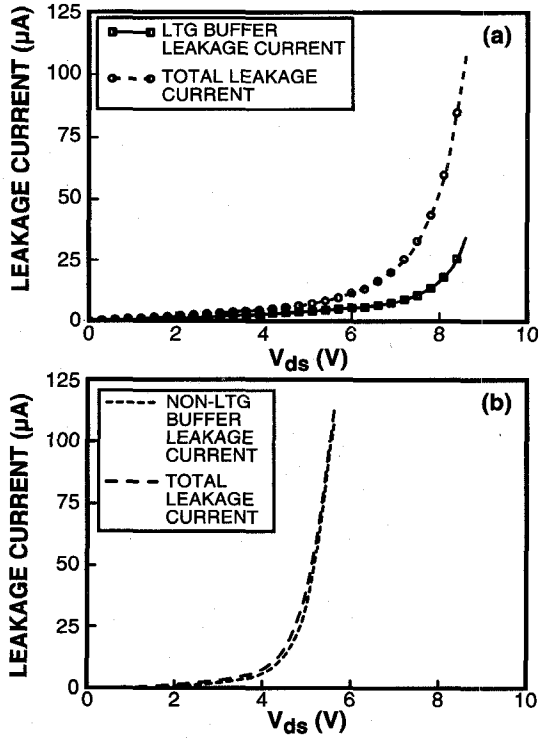

Fig. 4 Plot of the total channel breakdown current and the buffer leakage current for a typical 200-μm device from (a) an LTG-buffered and (b) conventional-buffered pHEMT wafer. Gate-source voltage is -1.0 volts.

and a corresponding conventional-buffered control wafer were measured to determine the drain-souce breakdown voltage (at Ids=100 μA) with a gate voltage of -1.0 volt. Fig. 2 illustrates a histogram of the channel breakdown voltage distribution for an LTG-buffered and a conventional-buffered pHEMT wafer. The LTG-buffered wafers achieved a channel breakdown voltage increase of 45% over that of the control pHEMT wafers.

Additional verification of the improved current-confining ability of the LTG GaAs buffer was provided by separating the drain-source leakage current into the contributions from the buffer-only leakage and any surface current leakage. As shown in Fig. 3., this measurement is performed using an HP 4142B semiconductor parameter analyzer and simulates the conditions that the device is likely to experience when biased near class AB operation for high efficiency operation. The gate-source and gate-drain breakdown voltages were measured separately and found to have a value of 10 volts for a 100-μA current. By calculating the difference between the gate-source current and the total drain-source current, Ids , the buffer leakage component was found. Fig. 4 illustrates the plot of the total channel breakdown current and the buffer current for a typical 200 μm device from an LTG-buffered wafer and a control wafer. As shown in the plot, the wafer with the conventional buffer layer has a channel breakdown dominated almost exclusively by the buffer leakage. In contrast, the buffer leakage current of the LTG-buffered device was only 30% of the total channel leakage current. This indicates that the LTG-buffered device is dominated by a surface breakdown effect, whereas the non-LTG-buffered wafer is limited by channel breakdown. From this data, it is expected that placement of the LTG GaAs buffer layer still closer to the channel would decrease the buffer leakage current to essentially zero.

Some of the more pertinent dc-characteristics are given in Table I. Pinchoff voltages were near -0.4 volts with peak normalized transconductance values of 700 mS/mm for both the LTG-buffered and the conventional-buffered pHEMT wafers. This was verification that the presence of the LTG buffer is not adversely affecting the high mobility InGaAs channel layer.

IV. RF CHARACTERIZATION

The small-signal RF characteristics of 200 μm and 400 μm total gate-periphery devices were measured using on-wafer microwave probes. Fig 5 illustrates the transducer gain S_{21}, maximum stable gain, MSG, and short-circuit unity current gain, h_{21} of 15 randomly chosen 200-μm devices from an LTG-buffered pHEMT wafer. The devices exhibited f_t-values ranging from 90 - 100 GHz and MSG-values greater than 16 dB at 20 GHz. Excellent small-signal uniformity across the 3-inch wafer was observed, thus confirming the uniformity of LTG GaAs deposition.

In order to perform large-signal power evaluations, approximately 12 devices consisting of 200-μm and 400-μm gate-peripheries were selected and packaged into 0.005-inch thick alumina microstrip circuits.

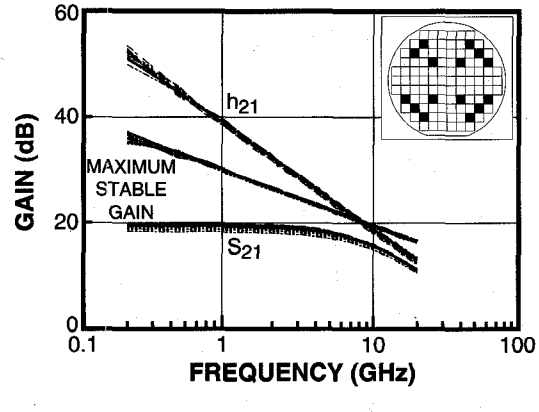

Fig. 5 The transducer gain (S_{21}), maximum stable gain (MSG), and short-circuit unity current gain (h_{21}) of 15 randomly chosen 200-μm total gate-periphery devices from an LTG-buffered pHEMT wafer.

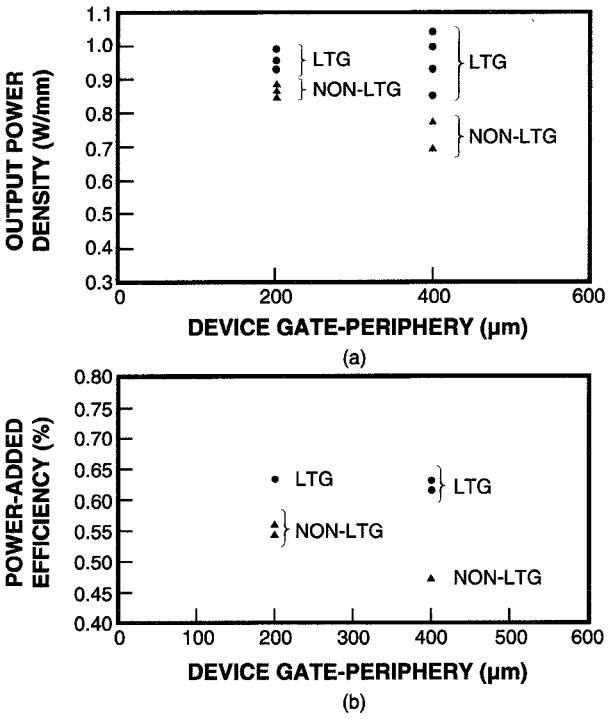

Fig. 6 (a) The optimum power output, and (b) the optimum power-added efficiency of LTG-buffered and conventional-buffered pHEMTs at 20 GHz.

For these tests, an automated active loadpull measurement system with full error-corrected power and reflection coefficients was utilized to evaluate the power output and power-added efficiency at 20 GHz[4]. Fig. 6 illustrates the power output performance under optimum power tuning conditions. At 20 GHz, the normalized power densities for the conventional-buffered pHEMT wafer ranged from 0.7 - 0.87 W/mm for a drain bias of 5.0 - 5.9 volts. The LTG-buffered wafer achieved normalized power densities ranging from 0.95 - 1.04 W/mm for similar drain biases. These results represent a 12% increase in output power of the LTG-buffered wafers when contrasted with the conventional-buffered wafers. The power-added efficiency at 20 GHz was also measured and found to be (under optimum efficiency tuning conditions) 55 % at a power density of 0.7 W/mm for the control wafer and 63% at 0.93 W/mm for the LTG-buffered wafer. Table I summaries typical characteristics and RF performance of the conventional-buffered and LTG-buffered pHEMTs.

SUMMARY

An improved GaAs power pHEMT structure has been presented. This structure utilizes an LTG GaAs layer instead of the conventional buffer layers currently used by device manufacturers. PHEMT devices using this new buffer have shown a 45% increase in channel breakdown voltage, a 12% increase in power output, and an 8-percentage-point increase in power-added efficiency at 20 GHz when contrasted with conventional-buffered pHEMTs of similar topology. A record 63% power-added efficiency was measured at 20 GHz.

Table I

PARAMETER	CONTROL pHEMT	LTG-BUFFERED pHEMT
Transconductance	650-750 mS/mm	650-700 mS/mm
Channel Breakdown Voltage	5.5-6.0	8.5-9.0 volts
Power Density (20 Ghz)	0.7-0.87 W.mm	0.95-104 W/mm
Drain-Gate Breakdown Boltage	10 volts	10 volts
Power-Added Efficency (20 GHz)	55% @ 0.7 W/mm (Vds=5.5 V)	63% @ .93 W/mm (Vds=5.5 V)
RF Gain (20 GHz)	9.4 dB @ 0.87 W/mm	10.5 dB @ .93 W/mm
Small-Signal RF Gain (MSG at 20 GHz)	17 dB	16 dB
f_T	100 GHz	100 GHz

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